Call for REGISTRATION

EPTC 2019 **Registration details** can be found here

EPTC 2019 **Advance program** can be found here

The 21st Electronics Packaging Technology Conference (EPTC 2019) is an International event organized by the IEEE RS/EPS/EDS Singapore Chapter and sponsored by IEEE Electronics Packaging Society (EPS). EPTC 2019 will feature keynotes, a panel session, Invited talks, technical sessions, short courses, forums, an exhibition, social and networking activities. Since its inauguration in 1997, EPTC has developed into a highly reputed electronics packaging conference in the Asia-Pacific and is well attended by experts in all aspects of electronics packaging technology from all over the world. EPTC is the flagship conference of IEEE EPS in Region 10.

EPTC 2019 Program includes technical presentations contributed by distinguished speakers from industry, academia and research institutions. A complimentary conference banquet will be held in Marina Bay Sands, the conference hotel. For easy access to the conference venue and a comfortable stay in Singapore, we have engaged with Marina Bay Sands to offer specially-discounted room prices via here

The Program highlights are as follows:

KEYNOTES

INNOVATIONS IN ELECTRONIC PACKAGING FOR COMPUTE AND COMMUNICATION
DR. RAM VISWANATH, VP, INTEL

ENABLING THE BUILDING BLOCKS FOR NEXT GENERATION OF ELECTRONICS PACKAGING
GLEN MORI, MANAGING DIRECTOR , AMAT

Keynotes details can be found here

PROFESSIONAL DEVELOPMENT COURSES

The conference registration includes a complimentary half-day Professional Development Course (PDC) among five listed below, which will be conducted by leading experts in the field in the morning of 4th December 2019.

- Prof. Mervi Paulasto-Kröckel; Aalto University, "Power Electronics Packaging for Automotive Application"
- Dr. John H Lau; Unimicron Technology Corporation, "Fan-Out Wafer/Panel-Level Packaging and Heterogeneous Integrations"
- Prof. Xuejun Fan; Lamar University, "Reliability Mechanics and Modeling for IC Packaging - Theory, Implementation and Practices"
- Prof. Y. P. Zhang; Nanyang Technological University, "Antenna-in-Package (AiP) Technology for Millimeter Wave Systems"

- Prof. Chris Bailey, University of Greenwich, "Co-Design/Modeling and Additive Manufacturing for Electronics Packaging"

PDC details can be found here

All PDCs being presented at the 21st EPTC, in Singapore, have been approved to receive 0.35 Continuing Education Units (CEUs) or 3.5 Professional Development Hours (PDHs). CEUs and PDHs are recognized internationally by employers for continuing professional development as a formal measure of participation and attendance in "non-credit" self-study courses, tutorials, symposia, and workshops.

PANEL SESSION

Packaging Challenges & Opportunities for 5G Applications

Dr. Haley Fu, Director, iNEMI. (Moderator)

Dr. Seung Wook Yoon; Corporate VP, Package Technology Planning, Test & System Package, Samsung Electronics.

Prof. Y. P. Zhang; Nanyang Technological University.

Mr. Kikuchi, Shunichi; CVP, Fujitsu Advanced Technologies Limited.

Dr. Toshihisa Nonaka; Director, Hitachi Chemical Co. Ltd.

Mr. Erkko Helminen; Snr. Manager, TTM Technologies.

Dr. Gokul Kumar, Snr Manager, packaging design and development, Micron.

Panel details can be found here

INVITED PRESENTATIONS

- Dr Curry Chen, ASE Global, "Development of multi-chip integration non-molded 2.5D IC Packaging Technology"
- Prof Jeffrey Suhling, Auburn University, "Reduction of Aging Induced Reliability Degradations Using SAC+X Lead Free Solders"
- Dr Gokul Kumar, Micron, "Memory-Centric Design Challenges for Flash products"
- Prof Yogendra Joshi, Georgia Institute of Technology, "Cooling of high power microelectronic components using flow boiling"
- Mr. Murayama Kei, Shinko Electric Industries, "Effects of trace element on electro-migration of flip chip interconnect between Cu pillar and Sn-Bi alloy system"
- Prof SB Park, State University of New York, "Importance of Warpage Engineering in the era of Heterogeneous Integration"
- Dr Szu Huat Goh, Global Foundries, "Evolution of Fault Isolation Techniques for Product Failure Analysis"
- Dr Sia Choon Beng, Formfactor, "Highly Accurate, Efficient and Reliable Silicon Photonics Wafer-Level Test and Characterization"
- Dr Takenori Fujiwara, Toray Industries, Inc. "Development of Novel Polymer Materials for Advance Packaging"
- Dr Murali Sarangapani, Heraeus Singapore, "Micro-Interconnects: Signal Integrity in 5G applications."

- Mr. Shunichi Kikuchi, Fujitsu Advanced Technologies Limited, "System Packaging Solutions for High Performance Computing in the Era of 5G/IoT"
- Dr. Luan Jing-En, STMicroelectronics, "Virtual prototyping for electronic packaging development, dream or reality?"
- Mr. Favier Shoo, Yole Development, "Market and Technology Trends of Advanced Packaging, Fan-Out Packaging"
- Mr. Xue Ming, Infineon, "What is new for the fast learning of IC Reliability - Advanced Defect Learning, Package Structural Testing, & Reliability modelling by HPC"
- Mr. Premachandran CS, Globalfoundries, "A comprehensive Reliability assessment on 2.5D and 3D Integration"
- Dr Dongshun Bai, Brewer Science, "Material Advancement for Heterogenous Integration"
- Prof Sarah Kim, Seoul National University of Science and Technology, "Plasma process optimization for Cu bonding integration using the design of experiment technique"
- Dr Yasuhiro Morikawa, Ulvac, "Manufacturing Technology Solution of Small Via for Heterogeneous Integration"
- Dr Daniel Rhee Min Woo, "Novel MEMS based Lateral Contact Probing Method for Fine Pitch Micro-bumps for High Bandwidth Memory (HBM) Testing", Samsung.
- Dr. Yu-Po Wang, "Innovative Package for 5G Era", SPIL.

Invited Presentations details can be found here

The content of the invited presentations from distinguished industry speakers will not be published in the conference proceedings and only conferee will have the privilege of hearing from these industry speakers.

WORKSHOP

Heterogeneous Integration Roadmap (HIR)

The roadmap offers professionals, industry, academia and research institutes a comprehensive, strategic forecast of technology over the next 15 years. The HIR also delivers a 25-year projection for heterogeneous integration of emerging devices and materials with longer research-and-development timelines. This HIR Workshop will be conducted by Dr William Chen, Dr Bill Bottoms, and other experts in the field.

CONFERENCE TOPICS

- 2.5D, 3D and TSV Processes
- Advanced FA and Reliability for IC Packages
- Advanced Materials and Processing
- Advancement in Solder Joint and Reliability
- Die Attach and Sintering Technologies
- Electrical Simulation and Characterization for Advanced Packaging.
- Hybrid Bonding
- LED and Photonic Packaging
- Liquid Cooling and Micro-Fluid Technology
- Materials Challenges for Power Module Packaging
- MEMS Sensors and IoT Packaging and Processes
- Mold Compound Characterization and Processing
- New Interconnects for 3D and Heterogeneous Integration
- Next Generation Wirebonding & Characterization
- Power Module Assembly and Technologies

- Printed Electronics
- RF, 5G and mmWave Packaging
- Silicon and Glass Interposer Processing
- Thermal Simulation and Characterization for IC and Emerging Packages
- Thermal & Thermo-mechanical Simulation for Advanced Packages
- Wafer Fan-Out Processes and Characterization.

Mr. Wui-Weng WONG, *General Chair*
Dr. Eric J.R. PHUA, *Technical Chair*
https://www.eptc-ieee.net